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PREDICTING LONG-TERM FREQUENCY DRIFT IN FET OSCILLATORS USING DEVICE MODELING

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ABSTRACT

This paper analyzes, using device modeling, the long-term frequency drifts observed in GaAs FET oscillators stabilized by a dielectric resonator. The dominant contributor to the long-term frequency drift was found to be the change in gate-to-source channel capacitance of the FET. Excellent correlation between theory and measured data was achieved. The method is general and, to our knowledge, is the first analytical effort to explain long-term frequency drifts in this type of oscillator.

INTRODUCTION

High-stability sources are used in analog and digital microwave communication systems. The frequency stability of 20 or 30 ppm needed to meet the FCC objectives is achieved generally by using a phase-lock source. In the last couple of years, the free-running dielectric resonator oscillators (DRO) have appeared as substitutes for the phase-lock sources. When a GaAs FET is used as the active device, long-term frequency drifts exceeding the requirements were observed in these oscillators.

The investigation of the long-term frequency drift was undertaken using S-parameters and the GaAs FET model. The method is quite general and can also be used for oscillators using bipolar devices.

DIELECTRIC RESONATOR AND GaAs FET MODEL

A dielectric resonator model was derived from transmission measurements in a 50-ohm microstrip fixture. The resonator was placed on a thin quartz spacer above the substrate. The model is valid for a narrow band around the resonance frequency (eg, 10.742 to 10.762 GHz) of the dielectric resonator.

The S-parameters of several GaAs FETs were measured over 2 to 12 GHz. The equivalent circuit parameters were calculated using Liechti's MESFET model and Super-compact.

FET AS AN AMPLIFIER/OSCILLATOR

When the GaAs FET is used as an amplifier, for a ±10-percent variation in FET parameters, only a ±0.3-dB maximum change in the maximum available gain of 10 to 12 dB is observed (figure 1). This small change in gain can be easily compensated. Using the same FETs in high-stability oscillators (20 ppm), however, results in a larger than expected frequency drift. Parallel feedback DROs were designed with feedback coupling through a dielectric resonator. Several of these oscillators were placed on a long-term frequency stability test. The RF output power, frequency, DC bias currents, and voltages were monitored over time. To reduce the load pulling and measurement system effects, a 10-dB pad and an isolator were connected to the output.

OSCILLATOR DRIFT ANALYSIS

Frequency drift resulting from intrinsic device parameters was considered. Individual parameters (C_{gs}, g_m, C_{gd}, C_{dc}, R_{ds}, and R_i) were allowed to vary up to a maximum of 10 percent in the direction expected by the device physics. The frequency drift caused by the 10-percent variations of C_{dc}, R_{ds}, and R_i was found to be insignificant (2 to 3 ppm). However, a 10-percent variation of C_{gs}, C_{gd}, and g_m resulted in a 20- to 100-ppm frequency drift (figure 2), with the largest contribution to the frequency drift caused by channel capacitance, C_{gs}. Transconductance g_m and C_{gd} cause smaller drift, opposite to each other that tends to cancel. A 10-percent variation of all these paremeters could cause up to 135-ppm long-term drift in frequency. From early reliability studies(1), measured long-time drift data for g_m and V_{gs} on a 1-watt power FET at 12 GHz is available. This data along with device physics was used to predict time dependence of transconductance and channel capacitances in an FET.

Transconductance Analysis

The behavior of g_m with time, t, and channel temperature, T, can be described as:

$$g_m(t,T) = g_{m1}(T) + g_{m2}(T)e^{-\alpha(T)\cdot t} \quad [1]$$

where the time, t, is in days and channel temperature, T, is in °C. $g_m(0,t)$ is the value of transconductance in data sheets.

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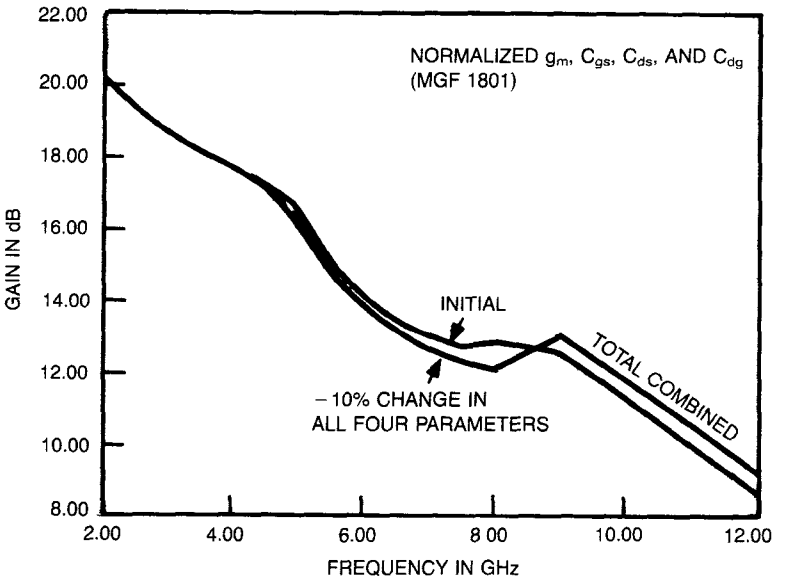


Figure 1. Change of Maximum Available/Stable Gain With g_m, C_{gs}, C_{ds}, and C_{dg}.

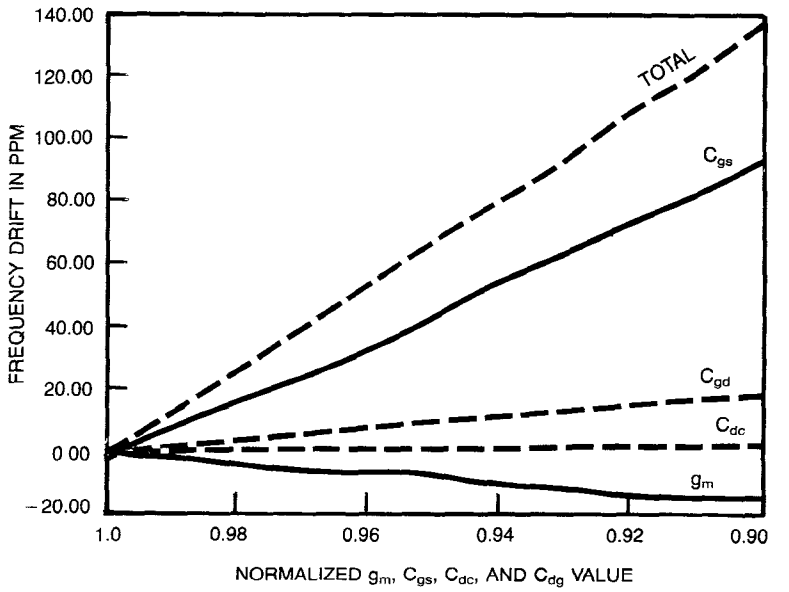


Figure 2. Effect of FET Parameters on Long-Term Drift of DROs (MGF 1801).

Parameter $\alpha(T)$ is the channel degradation factor, defined as:

$$\alpha(T) = \alpha_0 + \alpha_1 e^{-\alpha_2 T} \quad [2]$$

α_0, α_1, and α_2 are constants for the specific device and can be calculated from measured data. g_{m1} and g_{m2} can be expressed as:

$$g_{m1}(T) = g_{m10} - g_{m11} \cdot T \quad [3]$$

$$g_{m2}(T) = g_{m20} + g_{m21} \cdot e^{\gamma T} \quad [4]$$

where γ and g_{mIJ} are again constants and found from the measured data.

Channel Capacitance Analysis

The behavior of channel capacitance can be calculated using metal-semiconductor junction theory and the hyperboloid junction doping profile generally used in MESFETs. These channel capacitances, C_{gs} and C_{gd}, have the following relationship with applied voltage, $V_a(t)$.

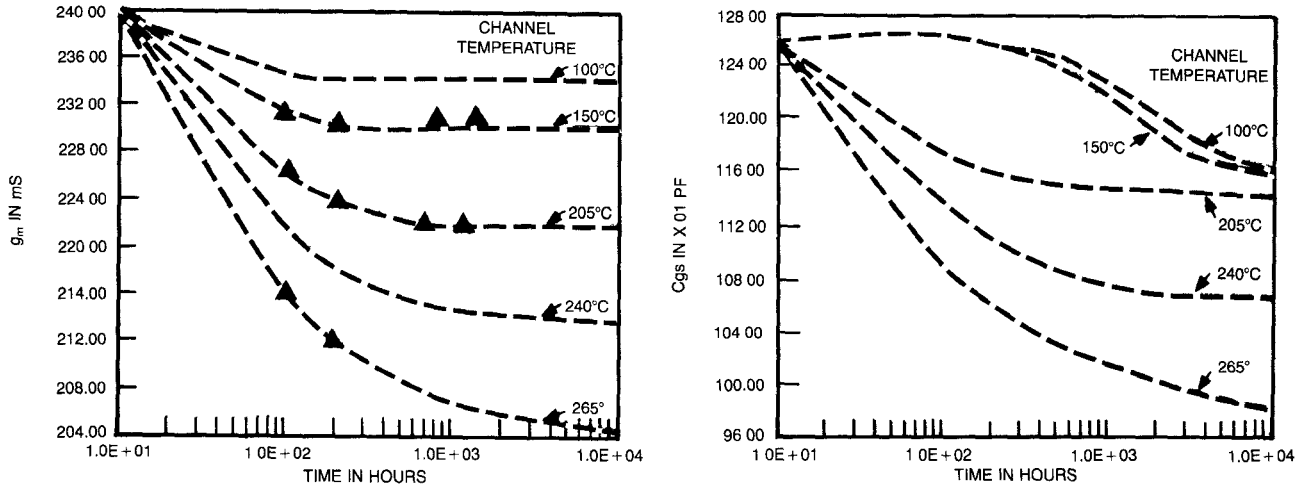
$$C = \frac{A \cdot \epsilon_s}{K_2 \cdot [\phi_1 - V_a(t)]} = K_3/[\phi_1 - V_a(t)] \quad [5]$$

where $K_2 = (2\epsilon_s/qK_1)$ = constant, K_1 is a constant
$K_3 = A \cdot \epsilon_s/K_2$ = constant, ϕ_1 = built-in voltage
A = area of the contact, q = electron charge
$\epsilon_s = \epsilon_r \epsilon_0$, ϵ_r = 13.1 for GaAs

The constant K_1 can be found by knowing the doping density, N_d and depletion width, W_d of the MESFIT

$$K_1 = N_d W_d = \sqrt{\frac{2\,\epsilon_s\,N_d\,(\phi_1 - V_a)}{q}} \quad [6]$$

The relations [1] to [6] describe the time and channel temperature dependence of g_m and C_{gs} for the large GaAs FET quite well (figure 3). The long-term behavior of g_m is predicted by the model to an accuracy of about 2 percent. The model is scaled to the smaller device, as used in DROs, with output power of 23 dBm. Using this data, frequency drift of DROs for different channel temperatures is calculated over time (figure 4). It is observed that for devices operating at low channel temperatures of 100° to 150°C, initial device current increased by as much as 10 percent(2), which results in a lowering of oscillation frequency. After a few days, the device current decreases and follows the more typical pattern, resulting in an increase of oscillation frequency of the DRO. At high channel temperatures (265°C), the device shows a large initial drift and continues to drift, almost like a runaway effect, and takes a long time to slow down. The model predicts the observed behavior and general trends of long-term frequency drifts quite well, with good agreement between the calculated and measured data.



a. g_m

b. C_{gs}

Figure 3. Drift of g_m and C_{gs} With Time and Channel Temperature (▲▲▲ Measured, — — — Calculated).

CONLUSION

The analysis shows that to achieve a high long-term frequency stability of 20 ppm or better, the device parameters should not change more than 1.5 percent. This is equivalent to 0.2- to 0.3-percent change in S-parameters of the devices and is very difficult to measure directly using network analyzer or similar measurement system.

When the device is biased to deliver output powers close to its maximum power capability, the drift mechanism is accelerated. (See high temperature curves in figure 4.) It is recommended that the GaAs FETs should be operated several decibels backed off from their maximum power capability. This would allow the required stability to be realized using FET oscillators. The oscillator output can be amplified for higher output power levels as necessary.

ACKNOWLEDGMENTS

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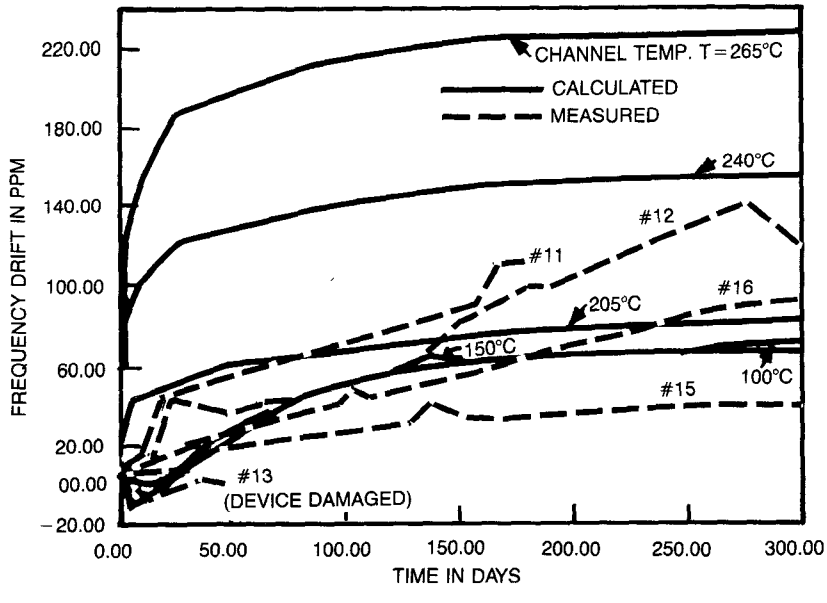

Figure 4. Long-Term Frequency Drift of DRO From Analysis and From Measurements.